REMARKS/ARGUMENTS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 14-18 are presently active, Claims 1-13 having been previously canceled without prejudice, Claims 14 and 16 having been amended, and Claims 17 and 18 having been added by way of the present amendment. No new matter has been added.

In the outstanding Office Action, Claims 14-15 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Lattimore et al (U.S. Pat. No. 5,831,896) in view of Rapp (U.S. Pat. No. 4,189,785).

Firstly, Applicant acknowledges with appreciation the courtesy of Examiner Le to discuss informally changes to the specification regarding Figure 8 and the third embodiment. No agreement was reached during these discussions as to whether such changes raised an issue of new matter, pending formal submission of the changes and arguments therefore.

M.P.E.P. § 2163.07 indicates that an amendment to correct an obvious error does not constitute new matter where one skilled in the art would not only recognize the existence of the error in the specification, but also the appropriate correction. In the present case, Applicant submits that the designation of the applied voltage $V + \Delta V$ in Figure 8 as originally filed and the associated discussion with regard to Figure 8 of $V + \Delta V$ in the specification was an obvious error, and that one skilled in the art would both recognize the existence of this error and the appropriate correction thereof.

For instance, in both the first and second embodiments of the present invention and in the corresponding Figures 1 and 3, a latch circuit 12 having complementary inverter circuits 21 and 22 is used to accept charge from the bit line BL when the word line WL is high. The specification at page 8, line 19, to page 9, line 8, discloses that:

> In the "1" data write mode, the power supply selection switch 33 is controlled to apply the second voltage VDD – ΔV, which is lower than the first voltage VDD by ΔV, to the source terminal of the P-type MOS transistor 22a from the second power supply 37. Thus, the power supply voltage applied to the second CMOS inverter circuit lowers and accordingly the threshold value of the input of the second CMOS inverter circuit 22 decreases. The output of the second CMOS inverter circuit 22, which has not yet been inverted, is decreased by voltage ΔV. In the first CMOS inverter circuit 21, the on-resistance of the N-type MOS transistor 21b increases and so does the output thereof. Consequently, the 5-transistor SRAM cells 11 are likely to cause an inversion operation for writing data "1."

Hence, when the WL goes high in the "1" data write mode, the applied load voltage to the inverter circuit 22 is ***decreased*** during the data "1" write mode. By decreasing the applied voltage, such as in Figure 1 where the applied voltage is decreased by application of VDD – ΔV to the source of MOS transistor 22a, the voltage existing at the midpoint between MOS transistor 22a and MOS transistor 22b is also decreased. Since the voltage at the midpoint is in turn applied to the gate of MOS transistor 21b in the complementary inverter circuit 21, a lowering of this voltage decreases the threshold value of the input of the inverter circuit 22, increases the on resistance of the MOS transistor 21b, increases the output of the MOS transistor 21b to the inverter circuit 22, and causes an inversion operation for writing data "1" to the latch circuit 12.

As such, the inversion operation of the latch circuit 12 is initiated on a ***reduction in voltage*** at the midpoint between MOS transistor 22a and MOS transistor 22b in Figures 1 and 3 and the first and second embodiments.

In original Figure 8, the application of an applied voltage VSS + ΔV to MOS transistor 22b would ***increase*** the resultant voltage at the midpoint between MOS transistor 22a and MOS transistor 22b, hence frustrating inversion and the writing of data "1" to the latch circuit 12. Thus, one of ordinary skill in the art would not only recognize that VSS + ΔV is erroneous,

but also would realize that VSS - ΔV should be applied to accomplish inversion and the writing of data "1" to the latch circuit 12.

Correspondingly, the specification in description of the third embodiment should have stated that VSS - ΔV was applied. Accordingly, the range of applied voltage would be reduced by the recited ΔV of about 5% to 30%,[1] and thus would range from 95% to 70% of VSS, as presently amended.

Secondly, Applicant respectfully traverses the 35 U.S.C. § 103(a) rejection based on a combination of Lattimore et al and Rapp for the following reasons.

Lattimore et al disclose a five transistor SRAM cell having a latch structure, and Rapp discloses a MOS memory array in which the source voltage is fluctuated. However, Lattimore et al merely disclose an example of a five transistor SRAM cell having a latch structure. In Rapp, the source voltage is fluctuated in every mode, such as a reading mode and a writing mode (for example, refer to the waveform indicated by line 32 in FIG. 3 of Rapp). Hence, the references individually or combination do not disclose or suggest the features defined in independent Claims 14 and 17 where a source voltage is switched to a first state at the "1" data writing time and switched to a second state in another mode, such as for example a read or standby mode.

As shown by example in replacement FIG. 8, the presently claimed invention is such that, in the 5-transistor SRAM cell 11 having one latch structure section formed by two CMOS inverter circuits 21 and 22 and the control transistor 13, the threshold of input of the second CMOS inverter circuit 22 is temporary decreased at the "1" data writing time. In this way, a stable "1"data writing is enabled without losing cell area reduction effect, decreasing write speed, compromising stability, or the like. That is, the 5-transistor SRAM cell 11 is configured such that the source voltage can be switched at the "'1" data writing time and when it is in

[1] Specification, page 16, lines 12-13.

another mode (for example, standby mode, data reading mode, or "0" data write mode).

Further, with regards to dependent Claims 15 and 18 where the source voltage to be fluctuated at the "1" data writing time is not fully swung, there is no fear that the write speed is decreased due to a source line. In Rapp, when attention is paid to the cell 22 at the time of writing "1" into the cell 18, Vcc is applied to the line 32 and V_{GUARD} is applied to the line 30, respectively. In a case where the relationship of voltage is as such, if "0" data is stored in the cell 22, the cell 22 cannot continue retaining the "0" data. As a result, "1"data is written. On the other hand, in Claims 15 and 18, where the voltage necessary for latch inversion of a selected cell is ΔV, the voltage ΔV is sufficiently smaller than the voltage which causes latch inversion in a non-selected cell, so that no error in writing occurs in the non-selected cell.

Further, in a system where a source voltage is changed at the reading time as in Rapp, (for example, refer to pulse 33 indicated by line 32 in FIG. 3 of Rapp), the change in the source voltage becomes a factor of noise with respect to a non-selected cell.

Hence, when the structure of a cell array is considered, the configuration described in Rapp presents practical noise problems.

Therefore, even when considering a combination of Lattimore et al and Rapp, a person skilled in the art without impermissible hindsight gained from the present specification and the advantages described therein would not conceive the structure of the present invention so as to realize a 5-transistor SRAM cell in which stable writing of data "1" is possible by fluctuating the source voltage at the "1" data writing time.

With no disclosure or suggestion of the above-noted features, it is respectfully submitted that independent Claims 14 and 17 and the claims dependent therefrom patentably define over the applied prior art.

Consequently, in view of the present amendment and in light of the above discussions, the outstanding grounds for rejection are believed to have been overcome. The application as amended herewith is believed to be in condition for formal allowance. An early and favorable action to that effect is respectfully requested.

Respectfully submitted,

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Amendments to the Drawings

The attached sheet of drawings includes changes to Fig. 8. This sheet which includes Fig. 8, replaces the original sheet including Fig. 8.

Attachment: Replacement Sheet.